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10/777,025	02/11/2004	Mario Di Ronza	INFN/0056	2196

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EXAMINER	
BRITT, CYNTHIA H	
ART UNIT	PAPER NUMBER
2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/777,025	RONZA ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-34 are pending in the present application.

Response to Arguments

Applicant's arguments with respect to claims 1-33 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary.

Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1- 5are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,862,703, Oonk in view of Deas U.S. Patent No. 6,065,090.

As per claim 1, Oonk substantially teaches a memory tester in accordance with the invention tests a random access memory device under test (DUT) comprising an array of rows and columns of memory cells, each having a separate row and column address. The tester provides a computer with enough information to determine how to efficiently allocate spare rows and columns for replacing rows and columns containing defective memory cells. As the tester tests each memory cell residing at a particular address within the DUTs, it writes a fail data bit into a corresponding address of an error capture memory (ECM) to indicate whether the memory cell is defective (column 2 lines 37-48). Not disclosed is the selective replacement of failed memory words, rows, and columns.

However, in an analogous art, Deas teaches the bits chosen for each defective location can be different for each slice. If there were a column error in one of the blocks then it would be preferable to use the full column address and a curtailed row address rather than the fill row address and a curtailed column

address. Both of these options (full row--partial column, and partial row--fill column) may be used. (Column 2 lines 46-53, Column 3 lines 8-24) Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the selective replacement of failed memory words, rows, and columns as taught by Deas with the tester of Oonk. One of ordinary skill in the art may find a motivation to combine prior art references in the nature of the problem to be solved. **Ruiz v. A.B. Chance Co.,** 357 F.3d 1270, 1276, 69 USPQ2d 1686, 1690 (Fed. Cir. 2004); Also **Pro-Mold & Tool Co. v. Great Lake Plastic Inc.**, 75 F.3d 1568, 1573, 37 USPQ2d 1626, 1630; **In re Huang**, 100 F.3d 135, 139 n.5; 40 USPQ2d 1685, 1688 n.5 (Fed. Cir. 1996). Both references are directed to the replacement of defective elements in a memory.

As per claim 2, Oonk teaches the computer reads the counts in one or more of the area fail counters when the test is completed to determine whether the DUT has any defective cells, and if so, which areas of the DUT's memory space contain the defective cells. In some cases, the computer will be able to determine whether and how to allocate spare rows and columns to replace DUT rows and columns containing defective memory cells on the basis of the count data alone. (Column 2 lines 49-63)

As per claim 3, Oonk teaches allocating a redundant row or column to a first row or column containing defective storage cells in preference over a second

row or column containing a lesser number of defective storage cells. (Column 2 lines 55-63)

As per claim 4, Oonk teaches replacing the defective storage cells of the second row or column with one or more redundant words. (Column 6 lines 29-59)

As per claim 5, Oonk teaches one redundant word replaces defective storage cells of at least two columns. (Column 7 lines 19-30)

As per claim 6, Oonk teaches activating a FAIL signal to indicate the memory device is not repairable if all defective cells detected cannot be replaced. (Column 5 lines 35-60)

Claims 7-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,862,703, Oonk in view of Applicant's admitted prior art.

As per claims 7, 9, and 13, Oonk teaches a memory tester in accordance with the invention tests a random access memory device under test (DUT) comprising an array of rows and columns of memory cells, each having a separate row and column address. The tester provides a computer with enough information to determine how to efficiently allocate spare rows and columns for replacing rows and columns containing defective memory cells. As the tester tests each memory cell residing at a particular address within the DUTs, it writes a fail data bit into a corresponding address of an error capture memory (ECM) to indicate whether the memory cell is defective (column 2 lines 37-48). Not disclosed by Oonk is that the method is preformed by a BIST and that a specific Row or Column test is preformed. However, AAPA discloses prior art methods which teach all of the above (AAPA [0012-0014]) Therefore, it would have been

obvious to a person having ordinary skill in the art at the time this invention was made to have used the above methods with the method of Oonk in order to provide a test and repair method on chip.

As per claim 7,AAPA teaches the method is performed as part of a built-in self test (BIST) of the memory device. AAPA [0012]

As per claim 8, AAPA teaches the BIST serves multiple memory devices with embedded and shared redundant elements. AAPA [0012]

As per claim 9, AAPA teaches detecting defective storage cells comprises conducting a column test. AAPA [0012]

As per claim 10, AAPA teaches, wherein conducting the column test comprises identifying and storing addresses of columns having greater than a threshold number of defective storage cells. AAPA [0012-0014]

As per claim 11, Oonk teaches the column test comprises overwriting addresses of columns having a first number of defective storage cells with addresses of columns having a second number of defective storage cells, wherein the second number is greater than first number. (Column 2 lines 5-26)

As per claim 12, AAPA teaches detecting defective storage cells comprises conducting a row test. AAPA [0012]

As per claim 13, AAPA teaches detecting defective storage cells comprises conducting a row test. AAPA [0012]

As per claim 14, Oonk teaches conducting the row test comprises identifying and storing addresses of rows having greater than a threshold number of defective storage cells. AAPA [0012-0014]

As per claim 15, Oonk teaches replacing defective storage cells of rows having greater than the threshold number of defective storage cells with redundant words. (Column 2 lines 5-26)

Claims16-21, 23-25, and 27-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,795,942 Schwartz in view of

As per claims 16 and 34, Schwartz teaches a self-repairing memory device comprising: at least one array of storage cells arranged in columns and rows, with each row comprising multiple words; at least one of redundant row or column elements for replacing rows or columns containing defective storage cells; and at least one block of redundant word elements for replacing words containing defective storage elements without replacing the entire rows containing the words being replaced. (Column 2 line 42 through column 3 line 3) Not explicitly taught by Schwartz is Not disclosed is the selective replacement of failed memory words, rows, and columns.

However, in an analogous art, Deas teaches the bits chosen for each defective location can be different for each slice. If there were a column error in one of the blocks then it would be preferable to use the full column address and a curtailed row address rather than the fill row address and a curtailed column address. Both of these options (full row--partial column, and partial row--fill column) may be used. (Column 2 lines 46-53, Column 3 lines 8-24) Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used the selective replacement of failed memory

words, rows, and columns as taught by Deas with the memory device of Schwartz. One of ordinary skill in the art may find a motivation to combine prior art references in the nature of the problem to be solved. **Ruiz v. A.B. Chance Co.,** 357 F.3d 1270, 1276, 69 USPQ2d 1686, 1690 (Fed. Cir. 2004); Also **Pro-Mold & Tool Co. v. Great Lake Plastic Inc.**, 75 F.3d 1568, 1573, 37 USPQ2d 1626, 1630; **In re Huang**, 100 F.3d 135, 139 n.5; 40 USPQ2d 1685, 1688 n.5 (Fed. Cir. 1996). Both references are directed to the replacement of defective elements in a memory.

As per claim 17, Schwartz teaches built-in self repair (BISR) circuitry configured to replace at least one of a row or column containing one or more defective storage cells with a redundant row or column and to replace at least one word containing one or more defective storage cells with a redundant word without replacing the entire row containing the at least one word. (Column 2 line 42 through column 3 line 3)

As per claim 18, Schwartz teaches the built-in self repair (BISR) circuitry is configured to allocate redundant row or column elements to rows or columns containing defective storage cells based on the number of defective storage cells contained therein. (Column 2 line 42 through column 3 line 3)

As per claim 19, Schwartz teaches the built-in self repair (BISR) circuitry is configured to replace, with redundant word elements, defective storage cells contained in rows or columns not allocated redundant row or column elements. (Column 2 line 42 through column 3 line 3)

As per claim 20, Schwartz teaches: the at least one array of storage cells comprises multiple arrays of storage cells; and at least two of the arrays of storage cells share the block of redundant word elements. (Column 2 line 42 through column 3 line 3)

As per claim 21, Schwartz teaches the at least one array of storage cells comprises multiple arrays of storage cells; the at least one of redundant row or column elements for replacing rows or columns containing defective storage cells comprises redundant row elements and redundant column elements; and each array of storage cells is provided with at least one BISR circuit. (Column 2 line 42 through column 3 line 3)

As per claim 23, Schwartz teaches the built-in self repair (BISR) circuitry comprises: row test circuitry; and a plurality of registers to store address of rows containing at least a first threshold number of defective memory cells, as detected by the row test circuitry. (Column 2 line 42 through column 3 line 3)

As per claim 24, Schwartz teaches the built-in self repair (BISR) circuitry further comprises: column test circuitry; and a plurality of registers to store address of columns containing at least a second threshold number of defective memory cells, as detected by the row test circuitry. (Column 2 line 42 through column 3 line 3)

As per claim 25, Schwartz teaches the built-in self repair (BISR) circuitry comprises: column test circuitry; and a plurality of registers to store address of columns containing at least a threshold number of defective memory cells, as detected by the column test circuitry. (Column 2 line 42 through column 3 line 3)

As per claim 27, Schwartz teaches a memory built-in self test (BIST) circuit to identify defective storage cells. (Column 2 line 42 through column 3 line 3)

As per claim 28, Schwartz teaches a register for storing an address of a current column under test; a register for storing a number of faults in a current column under test. n column address registers for storing addresses of columns having defective storage cells; and n fault count registers for storing a corresponding number of faults in each column having an address stored in a column address register. (Column 2 line 42 through column 3 line 3,Column 5 lines 21-65 Fig 3) Deas teaches individual bits may be replaced by means of the partial memory engine. Since most faulty memory circuits contain relatively few errors (compared with the total number of memory cells) it is unlikely in most cases that there will be other defective bits in the same row or column with the same bit sequence of three or four bits in the least significant portion of the address. (Column 2 lines 12-53)

As per claim 29, Schwartz teaches a column threshold register; a comparator and decoder unit configured to store the address and corresponding defect count of the current column under test in a column address register and fault count register in response to determining the defect count of the current column under test exceeds a value stored in the column threshold register. (Column 2 line 42 through column 3 line 3,Column 5 lines 21-65 Fig 3)

As per claims 30, 32 and 33 Schwartz teaches the comparator and decoder unit is configured to store the address and corresponding defect count of the current column under test in a column address register and fault count register only if the corresponding defect count is not less than all other values stored in the fault count registers. (Column 2 line 42 through column 3 line 3,Column 5 lines 21-65 Fig 3)

As per claim 31, Schwartz teaches a row memory built-in self repair (MBISR) circuit comprising: a register for storing an address of a current row under test; a register for storing a number of faults in a current row under test. n row address registers for storing addresses of rows having defective storage cells; and n fault count registers for storing a corresponding number of faults in each row having an address stored in a row address register. (Column 2 line 42 through column 3 line 3,Column 5 lines 21-65 Fig 3) Deas teaches individual bits may be replaced by means of the partial memory engine. Since most faulty memory circuits contain relatively few errors (compared with the total number of memory cells) it is unlikely in most cases that there will be other defective bits in the same row or column with the same bit sequence of three or four bits in the least significant portion of the address. (Column 2 lines 12-53)

Claims 22 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,795,942 Schwartz.

As per claims 22 and 26,Schwartz substantially teaches the claimed self-repairing memory device comprising: at least one array of storage cells arranged

in columns and rows, with each row comprising multiple words; at least one of redundant row or column elements for replacing rows or columns containing defective storage cells; and at least one block of redundant word elements for replacing words containing defective storage elements without replacing the entire rows containing the words being replaced. (Column 2 line 42 through column 3 line 3) not disclosed by Schwartz is that the storage cells are dynamic storage cells and/or that the "bank of *non-volatile* storage elements to store addresses of at least one of rows or columns to be replaced with redundant rows or columns". However the examiner would like to point out that these specific types of memory would be merely a design choice as both nonvolatile memory and dynamic memory are well known in the art for these purposes. Therefore, it would have been obvious to a person having ordinary skill in the art at the time this invention was made to have used this type of memory.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 20040153925 A1 Ronza et al.

This patent teaches an integrated memory and method for testing an integrated memory is provided herein. In order to test an integrated memory having a main data memory with a plurality of data memory units, a data memory unit is addressed and input test data for testing the addressed data memory unit

are applied to the main data memory. The output test data are read out from the main data memory and compared with expected desired output test data in a self-test unit. Deviations detected during the comparison are buffer-stored in a redundancy analysis memory. These information items buffer-stored in the redundancy analysis memory are read out and transferred to a computing unit. In the computing unit, the defect positions in the output test data are identified, and *a repair strategy is determined by means of redundant rows and/or redundant columns and/or redundant words provided.* The redundant words required for the repair strategy are written to the redundancy analysis memory and activated.

Although the filing date in the US is not prior to applicant's EP filing date the EP filing date of Ronza et al. is prior to applicants EP filing date. Applicant is requested to carefully review this application.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 571-272-3815. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Cynthia Britt 1-20-07
Primary Examiner
Art Unit 2138